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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,403	09/26/2003	Ta-Chin Lin	TS01-1457	9152

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EXAMINER	
RAPP, CHAD	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,403	LIN ET AL.	
	Examiner	Art Unit	
	Chad Rapp	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,10,13-15,17-19,21-23,26 and 29-32* is/are rejected.

7)☒ Claim(s) *4,8,9,11,12,16,20,24,25,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-32 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities:

On page 6, line15 "Real Tine" should be changed to "Real Time".

On page 8 lines 6 and 12 the performance indices 202 do not match with the 202 of figure 2 which are production indices.

On page 11 line 3 "ans" should be changed to "and".

On page 12, line 14 "os" should be "are".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 30-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 30, line 2-3 "the added considerations" should be changed to" added considerations". There is insufficient antecedent basis for this limitation in the claim.

In claim 30, line 3 "the same product" should be changed to "same product".

In claim 30, line 3, "the lot" should be changed to " a lot". There is insufficient antecedent basis for this limitation in the claim.

In claim 30, line 4 "said load board" should be changed to "a load board". There is insufficient antecedent basis for this limitation in the claim.

In claim 31, "said common constraint" should be changed to "a common constraint".

In claim 31, "the PROMIS" should be changed to "a PROMIS". There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 8 and 24, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

5. If the above problems are fixed then claim 32 would have allowable subject matter.

Allowable Subject Matter

6. Claims 4, 8, 9, 11, 12, 16, 20, 24, 25, 27 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3, 7, 13-14, 17-19, 23 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al.(6,470,231) in view of Chen et al.

Yang et al. teaches the claimed invention(claims 1 and 17) substantially as claimed including a method for dynamic adjustment of priority and step procedures for determining effective lot dispatching for wafer and chip probing comprising:

a. Using two-phased, event driven dispatching system structure for said dynamic adjustment is taught as lot rank algorithm and lot assignment algorithm(col. 4 lines 1-9);

b. Using said step procedures to choose lots that can utilize incorporated auxiliary apparatus without need for new setup is taught as when several tools are accessible the tool with the same product as the wafer is preferably used(col. 6 lines 61-62);

c. Solving dispatching conflict between wafer and package lots is taught as a method for dynamic dispatching(col. 2 lines 24-42).

Yang et al. teaches the above listed details of the independent claims 1 and 17, however, Yang et al. does not teach: providing for engineering lots capacity check in said step procedures and limiting tester's capability in product through use of common constraint system.

Chen et al. teaches :

a. Providing for engineering lots capacity check in said step procedures is taught as the machine capacity is checked(col. 8 lines 54-55);

b. Limiting tester's capability in product through use of common constraint system is taught as the step of determining capacity constraint(col. 3 line 26 and col. 1 line 60-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made or used to modify the teachings of Yang et al. with the teachings of Chen et al. because both patents deal with semiconductor manufacturing plants, dispatching and using lot

priorities to enhance the production wafers. The capacity checks of machines in Chen et al. is very desirable because it can reduce time of production.

As to claims 2 and 18, Yang et al. teaches wherein two-phased, event driven dispatching system structure to comprise of lot rank and lot assignment is taught as lot rank algorithm and lot assignment algorithm(col. 4 lines 1-9).

As to claims 3 and 19, Yang et al. teaches wherein said lot rank to comprises of a lot rank priority formula for production wafers and packages and a lot rank for engineering lots is taught as the lot ranking algorithm(formula) is used to give each pending wafer an individual priority(col. 4 lines 5-7).

As to claims 7 and 23, Yang et al. teaches wherein said auxiliary apparatus includes tester, probe card and load board is taught as a probe card(col. 8 line 1).

As to claims 13 and 29, Yang et al. teaches wherein said dispatching conflict between wafer and package lots is avoided by having said step procedures make sure no wafer work in progress remains before allowing said package lots to be dispatched with the result of minimal changeovers is taught as the tool being in an idle state(no wip is processed in an idle machine)(col. 6 line 60).

As to claims 14 and 30, Yang et al. teaches wherein said package lots are treated as an engineering step procedure with a added considerations of dispatching a same product or same production type as a lot just tested and resource constraint of a load board is taught as test equipment(tools), when several tools are accessible the tool with same products as the wafer is preferably used(col. 5 lines 31-32 and col. 6 lines 61-62).

9. Claims 5, 6, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Chen et al. and further in view of Tai et al.

Yang et al. and Chen et al. teach the claimed invention see paragraph number 8 above.

As to claims 5 and 21, Tai et al.

Yang et al. teaches:

a. Wherein said lot assignment to comprises of exception lots, hot run, super hot run, normal lot is taught as super hot run , hot run, normal run and exception rule(col. 2 lines 36-39).

Tai et al. teaches:

b. Engineering lot dispatching rule with the object of being based on Master Production Schedule target to reduce setup time is taught as MPS varies to a degree as a function of lot dispatching to achieve the desired delivery date(col. 5 lines 21-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made or used to modify the teachings of Yang et al. with the teachings of Tai et al. because both patents deal with semiconductor wafers and reducing cycle time. Using MPS with a dispatching rule will achieve the targeted delivery (on-time-delivery) Also takes into effect various factors that need to be factored into the system to improve the dispatching and priority methods.

As to claims 6 and 22, Tai et al. teaches wherein dispatch in a test foundry can be affected by performance indices, special dispatch properties, auxiliary apparatus, tester constraints, and production mode is taught as performance indices and special processes. The performance of target achievement that reflects on the due date can be evaluated by developed indices.

10. Claims 10 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Chen et al. and further in view of Chi.

Yang et al. and Chen et al. teach the claimed invention see paragraph number 8 above.

As to claims 10 and 26, Chi teaches wherein said step procedures are expanded to consider different product lots in addition to same products to said utilize any same auxiliary apparatus without need for new set up is taught as to batch similar lots not identical but similar that can be processed to together on the same machine.

It would have been obvious to one of ordinary skill at the time the invention was made or used to modify the teachings of Yang et al. with the teachings of Chi because both patents deal with priority ratings of lots for the manufacturing of IC chips or wafers. The Chi patent checks similar wafers not same but similar to see if they can be processed at the same machine at the same time this would reduce time because the machine does not have to change because of a new recipe. This increases the utilization rate of the machine tool.

11. Claims 15 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Chen et al. and further in view of Yu et al.

Yang et al. and Chen et al. teach the claimed invention see paragraph number 8 above.

As to claim 15, Yu et al. teaches wherein said common constraint system is a PROMIS constraint system is taught as PROMIS which is a MES software suite and it has constraints which are identified(col. 1 line 51 and col. 9 lines 23-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made or used to modify the teachings of Yang et al. with the teachings of Yu et al. because both patents deal with manufacturing of lots. The Yu et al. patent uses PROMIS and its

constraints which effect the capacity of a machine. These constraints have to be figured in a dynamic dispatching method.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chad Rapp whose telephone number is (571)272-3752. The examiner can normally be reached on Mon-Fri 11:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (571)272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chad Rapp
Examiner
Art Unit 2125

cjr

LEO PICARD
SUPERVISORY PATENT EXAMINER
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